WHAT IS CLAIMED IS:

1. A memory device comprising:

a plurality of memory cells;

a decoding circuit coupled to the plurality of memory cells, wherein the decoding circuit generate a first and a second control signal based on an address; and

a power supply source coupled to selected ones of the plurality of memory cells based on the first control signal from the decoding circuit, wherein the power supply source provide one of a set of voltages based on the second control signal,

wherein the selected memory cells are programmed in accordance with the voltage from the power supply source.

2. A memory device comprising:

a plurality of memory cells;

a decoding circuit to generate a set of control signals based on an address; and

a plurality of bit lines that interconnect a subset of the plurality of memory cells,

wherein the bit lines are implemented as floating bit lines.

3. An integrated circuit memory system comprising:

a plurality of memory cells, each memory cell including a source, a drain, a control gate, and a floating gate, wherein the floating gate stores an electric charge, and wherein the memory cells are programmable by hot carrier injection; and

a supply source for supplying voltages to the source, the drain, and the control gate of selected ones of the plurality of memory cells, and for controlling the current flowing between the source and drain during programming, said wherein program is controlled by the current flowing in the memory cells.